Analysis and Optimization of Noise Response for Low-Noise CMOS Image Sensors

P. Martin-Gonthier, R. Molina, P. Cervantes, P. Magnan
ISAE, Université de Toulouse, 10 avenue E. Belin, 31055, Toulouse, France
philippe.martin-gonthier@isae.fr

Abstract — CMOS image sensors are nowadays widely used in imaging applications and particularly in low light flux applications. This is really possible thanks to a reduction of noise obtained, among others, by the use of pinned photodiode associated with a Correlated Double Sampling readout. It reveals new noise sources which become the major contributors. This paper presents noise measurements on low-noise CMOS image sensor. Image sensor noise is analyzed and optimization is done in order to reach an input referred noise of 1 electron rms by column gain amplifier insertion and dark current noise optimization. Pixel array noise histograms are analyzed to determine noise impact of dark current and column gain amplifier insertion. Transfer noise impact, due to the use of pinned photodiode (4T photodiode), is also measured and analyzed by a specific readout sequence.

Index Terms — CMOS Image sensors, dark current noise, pinned photodiode, low-light flux, Column gain amplifier

I. INTRODUCTION

CMOS image sensors are nowadays extensively used in commercial, scientific and space applications [1]-[3]. CMOS standard processes, which are developed for digital and mixed signal applications, are really attractive particularly because of their low power consumption, applicability for on-chip signal processing and large availability. Several ways have been explored to improve image sensor performances to a very high level and performances have been significantly enhanced with the use of CIS (CMOS Image Sensor) processes [4], [5]. Image sensors performances are described by key parameters which are Quantum Efficiency (QE), Conversion gain (CG), Dark Current (DC), Noise, Full Well Capacity (FWC), Photo-Response and Dark Signal Non-Uniformities (respectively PRNU and DSNU) and Modulation Transfer Function (MTF). Low light applications require low noise image sensors leading to noise optimisation of image sensors [6]. This noise reduction is really possible thanks to the use of pinned photodiode associated with a Correlated Double Sampling (CDS) readout. It reveals new noise sources which become the major contributors. This paper presents optimisations done to reach an input referred noise of 1 electron rms.

First part of section II describes a common readout circuit of a pinned photodiode imager. Then, noise model is depicted in relation with this common readout circuit. The last part of section II analyzes the noise contributor impacts and optimization means. Test vehicle with optimizations and associated noise measurement results are described in section III. In addition, a specific readout sequence is applied in order to show transfer noise impact due to the use of pinned photodiode on total noise. Section IV presents the conclusions and perspectives of this work.

II. NOISE MODEL OF CMOS IMAGE SENSOR

A. Common CMOS image sensor readout circuit

A common CMOS image sensor readout circuit architecture is shown in Fig. 1. It is composed of a photo-element: a pinned photodiode associated with a transfer gate; a reset switch allowing to reset the readout node; an in-pixel source follower which drives the signal from pixel to column readout circuit; a double sample and hold circuit for reference and integrated signal levels; an output stage allowing to drive the signal off chip or on chip for additional processing.

Fig. 1. Common readout circuit architecture of a CMOS image sensor

For a pinned photodiode pixel (4T), before the end of the integration time, the readout node is reset by the reset MOSFET (command signal RST). This level, called reference, is sampled and held (command signal SHR) in the column readout circuit in the reference channel via the in-pixel source follower (SF) and the row selection (RS) transistor. Then, the charge transfer from the photodiode to the readout node begins (signal TG). When the charge transfer is done, a voltage level corresponding to the integrated charges is sampled and held (command signal SHS) in the column readout circuit of the signal channel. Video signal voltage level results from the
subtraction of the two samples (reference and signal). This readout sequence allows reset noise cancellation by CDS sequence.

B. Common CMOS image sensor readout circuit noise model

The previous common CMOS image sensor readout circuit can be modeled by the synoptic diagram shown in Fig. 2, where \( \Phi_L \) is the photon flux, \( N_{DC} \) is the number of electrons corresponding to dark current integrated during photodiode integration time, \( \eta(\lambda) \) is the quantum efficiency, \( G_C \) is the conversion gain (depending on the sense node capacitance \( C_{SN} \)), \( A_1(f) \) is the first stage gain, \( SH(f) \) is the transfer function of the sample and hold circuit and \( A_2(f) \) is the output stage gain.

\[
V_{OUT} = (\eta(\lambda) \cdot \Phi_L + N_{DC}) \cdot G_C \cdot (C_{SN}) \cdot A_1(f) \cdot SH(f) \cdot A_2(f) \quad \text{where} \quad V_{OUT} \text{ is the output signal.}
\]

This synoptic diagram leads to the following transfer function:

\[
V_{OUT} = (\eta(\lambda) \cdot \Phi_L + N_{DC}) \cdot G_C \cdot (C_{SN}) \cdot A_1(f) \cdot SH(f) \cdot A_2(f)
\]

Finally, the input referred noise in electrons can be expressed by the following equation (3) when the sensor is in the darkness:

\[
\sigma_{TOT}(e) = \sqrt{\sigma_{SC}^2 + 2G_C^2 \sigma_{DC}^2 + 2A_1^2 \sigma_{SH}^2 + 2A_2^2 \sigma_2^2}
\]

C. Noise response optimization

As can be seen in the previous equation, different ways exist to minimize the noise response:

- Minimize in-pixel amplifier stage (source follower) and output stage (source follower). This minimization can be done by design optimizations (such as biases current, \( W \) and \( L \) MOSFET size or bandwidth settling).
- Increase conversion gain \( G_C \) by reducing sense (or readout) node capacitance. The conversion gain, which is the diffusion of the sense node, depends on the technology used. Sense node capacitance design with minimum layout rules leads to maximum conversion gain value.
- Minimize dark current value. Indeed, noise coming from dark current follows the Poisson law. The dark current value also depends on the technology used.
- Increase the gain of the readout chain. Indeed, if \( A_1 \) or \( A_2 \) increase, input referred noise will be lower. However, due to topological constraints, an enhanced amplifier cannot be implemented in-pixel. Only insertion of gain in the column can be implemented.

This paper is focussed on the noise optimization by reducing dark current noise and by increasing readout circuit gain with a column gain amplifier insertion. Therefore, the two last optimizations are presented in the next paragraph.

1) Dark current optimization

Dark current sources are shown on Fig. 4 [8]. There are mainly two sources of dark current in a photodiode: Firstly, current due to defect sites (a); and secondly current due to injection or off-leak (b). Only optimization on the defect sites is done in this paper.

\[
\begin{align*}
\sigma_{TOT}(e) & = \sqrt{\sigma_{SC}^2 + 2G_C^2 \sigma_{DC}^2 + 2A_1^2 \sigma_{SH}^2 + 2A_2^2 \sigma_2^2} \\
& = \sqrt{\sigma_{DC}^2 + 2G_C^2 \sigma_{DC}^2 + 2A_1^2 \sigma_{SH}^2 + 2A_2^2 \sigma_2^2}
\end{align*}
\]

Due to the differential readout sequence in order to obtain video signal (subtraction between reference and signal samples), noise power spectral densities from first stage source follower associated with sample and hold circuit and output stage source follower are doubled and reset noise is canceled leading to the simplified noise equation in darkness in volt rms (2):

\[
\sigma_{TOT}(V) = \sqrt{G_C^2 A_1^2 \sigma_{DC}^2 + 2A_1^2 \sigma_{SH}^2 + 2A_2^2 \sigma_2^2}
\]

Two locations of defect sites can be observed: defects between STI and photodiode and defects coming from SiSiO\(_2\) interfaces near the transfer gate transistor. CIS process offers optimised photodiode where defects between STI and photodiode are well passivated. Previous works show good results on dark current minimization due to the traps near the transfer gate transistor [8], [9]. By applying a negative bias during the integrating phase on the transfer gate, a significant dark current
reduction is observed. Indeed, during the transfer gate negative bias, the transistor is in accumulation and thermally generated electrons can recombine with accumulated holes.

2) Column gain amplifier insertion

The other way to reduce noise is to minimize the input referred noise by increasing the readout chain gain as can be seen in Fig. 5 and in [10], [11]. However, due to pixel topological constraints, no complex amplifier can be done in-pixel. Thus, the gain amplifier is inserted in the column where topological constraints are lower.

From Fig. 5, the input referred noise in electron becomes (4):

$$\sigma_{TOT} (e) = \sqrt{\sigma_{DC}^2 + \frac{\sigma_{AG}^2}{G_{C-i}^2 A_i^2} + \frac{\sigma_{SH}^2}{G_{C-i}^2 A_i^2} + 2 \frac{\sigma_{AG}^2}{G_{C-i}^2 A_i^2} + 2 \frac{\sigma_{SH}^2}{G_{C-i}^2 A_i^2}}$$

(4)

where $\sigma_{AG}$ is the noise corresponding to the in-pixel amplifier with new bandwidth due to column gain amplifier insertion, $\sigma_{AG}$ is the noise from the column gain amplifier inserted and $\sigma_{SH}$ is the noise coming from sample and hold circuits. This equation shows the input referred noise coming from the output stage and sample and hold circuit is reduced. In addition, noise from the in-pixel amplifier can be minimized by adjusting in-pixel amplifier biases and bandwidth.

III. TEST VEHICLE DESCRIPTION AND MEASUREMENTS

A test vehicle was designed in a CIS 0.18µm technology. It is a 256x256 pixel array with pinned photodiode (4T) and 7µm pixel pitch. The pixel array is composed of 5 sub-arrays:

- One sub-array with common readout circuit (without column gain amplifier inserted).
- Four sub-arrays named G1, G10, G20 and G30 with column amplifier inserted respectively with the following gain values: 1, 10, 20 and 30.

Fig. 6 shows a microphotography of the test image sensor designed.

![Microphotography of the test image sensor](image)

Noise measurements were done in order to evaluate impacts of dark current minimization and column gain amplifier insertion on the noise test image sensor. At first, dark current measurements were done to check its reduction when the transfer gate transistor was biased with negative voltage during integration time on the first sub-array of pixel with the common readout chain. Measurement results show a dark signal of 67electrons/s/pixel when no negative bias is applied to the transfer gate. This dark signal decreases drastically (64%) when a negative bias of -0.5V is applied. A value of 24electrons/s/pixel is measured. The dark signal reduction impact is depicted in Fig. 7 with the noise histogram of the sub-array with common readout circuit. Due to a tail in the various histograms, mean and median values are extracted. A slight noise reduction is observed between the two biases of the gate transfer. However, the other noise sources seem to be dominant.

![Input referred noise histogram](image)

Fig. 8 shows the noise histogram of sub-array G30 corresponding to a column amplifier inserted in the readout chain (gain of 30) with and without a negative bias applied to the transfer gate. A higher noise reduction is reached.

![Input referred noise histogram for readout circuit with column amplifier inserted (gain of 30) with and without negative transfer gate bias during integration time](image)

Table 1 shows the noise measurement results in electrons (rms) for the different readout chain types (common, G1, G10, G20 and G30) corresponding to the 5 pixel sub-arrays with negative bias applied to the transfer gate (-0.5V) during integration. These results show significant noise reduction when the gain of the inserted column amplifier is high.
However, when gain of the column amplifier is 1, an increase of the noise is observed. This is due to the insertion of the new noise source (corresponding to the inserted column amplifier) which is not reduced by the gain.

<table>
<thead>
<tr>
<th>READOUT CHAIN TYPE</th>
<th>COMMON</th>
<th>G1</th>
<th>G10</th>
<th>G20</th>
<th>G30</th>
</tr>
</thead>
<tbody>
<tr>
<td>MEAN VALUE</td>
<td>3.27</td>
<td>5.62</td>
<td>1.68</td>
<td>1.64</td>
<td>1.51</td>
</tr>
<tr>
<td>MEDIAN VALUE</td>
<td>2.66</td>
<td>5.07</td>
<td>1.25</td>
<td>1.20</td>
<td>1.10</td>
</tr>
</tbody>
</table>

Table 1: Noise measurements with the different readout chain (common, G1, G10, G20 and G30) with a negative bias of -0.5V for transfer gate during integration

As can be seen, a very low noise is reached for higher gains.

In order to determine where improvements can be made on the readout chain where column amplifier is inserted, other measurements were done. Specific chronograms, shown in Fig. 9, were applied. Fig. 9a shows the standard readout sequence of a pixel. Fig. 9b depicts the readout sequence with no integration. Indeed, a transfer is done before the sampling of the reset of the readout node leading to no integrated charge transferred. Fig. 9c illustrates the readout sequence with no integration and no transfer done between the reference (SHR) and signal SHS) samples.

Noise measurements from the sub-array G30 (column amplifier inserted in readout chain with a gain of 30) with negative bias applied to the transfer gate (-0.5V) during integration are illustrated in Fig. 10 and show the impact of the dark signal remaining and the transfer noise. The remaining dark signal has no impact on the noise. The transfer noise has only a slight impact on the total noise. This means the dominant noise sources are in the readout chain despite insertion of column amplifier with high gain. So, in order to reduce the total noise value, an enhanced optimization has to be made to reach sub-electron input referred noise.

IV. CONCLUSIONS

This work shows the noise impact of optimization of dark signal and column amplifier insertion in the common CMOS image sensor readout chain. Noise mean values of 1.51 electron rms are measured with a column amplifier gain of 30 and negative bias applied to the transfer gate (-0.5V) during integration. Specific readout sequences are applied to determine the impact of transfer noise and remaining dark signal on the total image sensor noise. Noise measurements show a slight impact of these parameters once optimization is done.

REFERENCES


