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Single Event Effects in 4T Pinned Photodiode Image Sensors

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Abstract—This paper describes how Single Event Effects (SEEs) produced by heavy ions disturb the operation of Pinned Photodiode (PPD) CMOS Image Sensors (CISs) in the frame of space and nuclear applications. Several CISs with 4T and 5T pinned photodiode pixels were exposed to ions with a broad Linear Energy Transfer range (3.3 to 67.7 MeVcm²/mg). One sensor exhibited Single Event Latchups (SEls). Physical failure mechanism and latchup properties were investigated. SEls are caused by the level shifters of the addressing circuits, which create frame perturbations - following which, in some cases, parts of the addressing circuits need to be hardened. In the second part of the paper, the effects of anti-blooming capabilities on the Single Event Transient effects (SETs) are analyzed. SETs in pixels can be partially mitigated by anti-blooming through the transfer gate and/or a dedicated transistor. This work also shows that the number of pixels disturbed by SETs can be reduced by using appropriate anti-blooming techniques.

Index Terms—CMOS, CIS, SEE, Heavy ions, Radiation effects, Pinned photodiode

I. INTRODUCTION

The space and nuclear radiation environments affect the behavior of microelectronic devices [1]. Since CMOS Image Sensors (CISs) use manufacturing processes similar to the ones used in microelectronic, they are affected by the effects induced by the radiation environment. Although the cumulative effects of radiation on these devices have been studied by the scientific community, there have been few studies on Single Event Effects (SEEs) in CISs for particles with a high Linear Energy Transfer (LET).

Both the space and the nuclear communities have already produced work on SEEs in CISs. The nuclear community uses sensors based on CIS, but it focuses on particles with relatively low LET [2], [3], or detectors involving high voltage [4]. Nevertheless, some recent articles have addressed the CIS issue in the Inertial Confinement Fusion (ICF) facilities, where the radiative environment is particularly harsh [5], [6].

In the space community, articles have reported various effects on 3T pixel CISs including Single Event Latchup (SEL) [7], Single Event Transient (SET) [7], [8], [9], Single Event Upset (SEU) and frame corruption [10], [11]. In our previous study on 3T sensors with conventional photodiodes [12], the devices stayed fully functional during exposure to ion beams, and only SETs were observed. The size of these SETs on the acquired frames depended neither on pixel design nor on operating voltages and seemed to be only defined by the diffusion of the charge carriers in the silicon. As far as we know, there have been few similar studies on SEEs in 4T pixels using a pinned photodiode [13], even though the charge collection, charge handling and saturation mechanisms can be different. This is why this work focuses on the effects of heavy ions on 4T pixel PPD CISs.

The first part describes the experimental setup used in all the experiments, the second part discusses the latchup effect obtained on one device tested. The last part discusses the SET effects and the effectiveness of anti-blooming with two different methods: through the transfer transistor, and through a dedicated anti-blooming transistor.

II. EXPERIMENTAL SETUP AND METHODOLOGY

In a commercial CIS, the digital functions located outside the pixel array (ADCs, on-chip sequencer, configuration registers, etc.) are similar to those that can be found in many CMOS ICs. SEEs in such digital circuits are already studied. Therefore, as in the study of 3T pixels [12], we decided to focus on the CIS electronic functions dedicated to photo-detection (the pixels) and to the elementary functions necessary to read the pixel values (address decoders and analog readout chain). With this method, SEEs in the imaging sub-circuits and SEEs in peripheral sub-circuits (found in highly integrated commercial CISs) can be investigated separately. The devices studied used 4T and 5T pixels (4T with an additional anti-blooming or global shutter transistor) with a differential analog output and off-chip sequencer. Side circuits include two digital address decoders (X and Y), and analog on-chip readout circuits with one Correlated Double Sampling (CDS) stage per column of pixels. These basic elements are the “minimum” requirement for addressing and extracting pixel signals and they are used in every more complex CISs.

All the sensors studied used a 0.18µm process dedicated to imaging applications. However, two different foundries were used. Both foundries apply the same design rules, but the pixel pitch and the doping profile of the epitaxial layer are different. Fig. 1 shows that the epitaxial substrates share a similar doping level of 10^{15}cm^{-3} but their thicknesses and the doping profiles of the high resistivity substrates are different. All the properties are summarized in Table I.

The CISs were exposed to different ions with LET ranging from 3.3 to 67.7 MeVcm²/mg at the Catholic University of
Fig. 1. P-type doping profiles of the epitaxial layer and the deep substrate for both foundries. Doping profiles are similar except for the depth (W_{epi}), which is greater for Foundry A, i.e., CIS1. A diagram of the Pinned PhotoDiode (PPD) and the Transfer Gate (TG) is included.

TABLE I

<table>
<thead>
<tr>
<th>Summary of the irradiated CISs</th>
</tr>
</thead>
<tbody>
<tr>
<td>Name</td>
</tr>
<tr>
<td>Foundry</td>
</tr>
<tr>
<td>Epitaxial layer (µm)</td>
</tr>
<tr>
<td>Format</td>
</tr>
<tr>
<td>Pixel pitch (µm)</td>
</tr>
<tr>
<td>Pixel type</td>
</tr>
<tr>
<td>PPD Area (µm²)</td>
</tr>
<tr>
<td>Max. electric output swing of the readout chain</td>
</tr>
<tr>
<td>Output of full well PPD</td>
</tr>
<tr>
<td>Gain of the readout chain</td>
</tr>
<tr>
<td>Output referred Charge to Voltage conversion Factor (CVF)</td>
</tr>
<tr>
<td>Full Well Capacity (FWC)</td>
</tr>
</tbody>
</table>

TABLE II

<table>
<thead>
<tr>
<th>Summary of the ions used for the irradiation</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ion</td>
</tr>
<tr>
<td>N⁵⁷⁺</td>
</tr>
<tr>
<td>N⁷⁺</td>
</tr>
<tr>
<td>Ar⁴⁺</td>
</tr>
<tr>
<td>Kr⁷⁺</td>
</tr>
<tr>
<td>Xe⁶⁺</td>
</tr>
</tbody>
</table>

Louvain-La-Neuve (UCL), in Belgium. The ion properties are summarized in Table II. All the data were acquired at normal incidence. Only the center of the electronic board carrying the CIS was exposed, to avoid radiation effects outside the chip.

III. RESULTS ON LATCHUP

One sensor (CIS1) exhibited two unusual phenomena when irradiated. During acquisition time, some random lines (2 per event) became black at random times. The effect always occurred with a stable white halo on the left part of the frames. Fig. 2 shows one of these lines with its halo. A second effect can be seen in Fig. 5. Some SETs spread along the entire line, forming white bands on the frames. All these effects remain while the device is powered up and can be cumulative. The CIS returns to normal operation after the irradiation, since the photoresponsivity (conversion gain and full well capacity) remains the same.

A. Latchup effects and localization

1) Halo and black line effects: First, the origin of the white halo, visible on the left of the black lines in Fig. 2, will be analyzed. It cannot be caused either by light, since the frames were taken in the dark, or by ions, since the spot is stable in several frames. The only remaining explanation is the collection of electrons generated in another part of the circuit. This generation occurs at a location where the electric field is strong enough to create hot carriers into the substrate, through impact ionization.

The MOS Field-Effect Transistor (MOSFET) used in the line-addressing subcircuit cannot create hot carriers, since nothing is visible in normal operation (without irradiation). In-pixel MOSFETs can create hot carriers only if current through the source-follower transistor is high [14], which is the case when the selection transistor gate is in a “high” logic state. The selection signal is the same for the entire line. As a result, a hot carrier effect should appear along the entire line, which was not the case in the experiment.

Hence, the hot carriers are not produced by the MOSFET inside the line-addressing circuits or in the pixels. There remains the possibility of the parasitic thyristor structure in the digital decoder section. When latchup is triggered, the thyristor...
generates hot carriers and near-infrared photons. These are usually observed by failure analysis tools such as static emission microscopy (EMMI) [15]. In the experiment, hot carriers and photons were produced by the parasitic structure if it was triggered by an incident ion. The carriers created diffuse in all directions, and are collected by neighboring photodiodes. Since the halo appears on the left part of the pixel array, the high current state must be located nearby. A circuit diagram is needed to locate the latchup precisely.

The block diagram in Fig. 3 shows sub-circuits specific to CIS1. The main difference with CIS2 and CIS3 is that the CIS1 decoders are supplied with 1.8V. However, the pixels need to be driven with 3.3V logic signals. As a result, level shifters were inserted between each decoder and pixel line, with a 3.3V inverter to drive all the line signals. In the circuit, the level shifters are responsible for the SEL for the following reasons:

- A high current condition can only be triggered by Single Event Latchup (SEL) in the 3.3V supplied sub-circuits (see section III-B).
- The level shifters are designed with the closest distance between NMOS and PMOS transistors allowed by the design rule manual. They are thus more sensitive to latchup than the inverters [15].

Moreover, the design constraint of one level shifter per line was not possible due to the dimensions of the transistors. As a result, the design included two close level shifters sharing the same well. Thus, the SEL in one level shifter affects the second, and two lines appear black in the frames.

When the two columns are connected (SelX and SelLU are high), the circuit behaves like a PMOS logic digital circuit. The first transistor (TBias) works as a current source controlled by the fixed bias. When input signals $V_{pix\,in}$ and $V_{pix\,lu}$ are different, the output signal is the result of a “winner-take-all” circuit for the lower input voltage (see Appendix A for the details on circuit behavior). In nominal operation, the sense node is discharged by photo-generated or ion-generated electrons. Thus, the pixel which receives the greatest photon flux has the lowest output voltage and controls the output potential $V_{out}$. In the event of very similar illumination levels, the output will be a trade-off between the two input levels. Therefore, there are two extreme cases:

- The latched column has a low-illumination pixel, and the value of the pixel being read will not be modified.
- The latched column has an illuminated pixel, and its value will replace the value of the pixel being read.

The process is repeated for all the columns being read, and for all the lines. In our case, images were taken in dark conditions. The effect is only visible if fixed pattern noise is observed. However, if an ion hits the latched column, the higher values of the SET profile will spread along all the lines because pixels surrounding the SET have a low illumination level. This creates the bands visible in Fig. 5. In the case of real images, white pixels on the latched column will spread along the entire line. Such events corrupt the output level until power is reset; as a result, the useful information is lost. Preventing this...
latchup requires insight into its properties, which are described in the next section.

Fig. 5. Consecutive frames obtained with CIS1 during irradiation. The band effect indicating the occurrence of SEL. It is only visible if an SET is present on the latched column (near Column 50 in this case).

B. Latchup cross-sections and properties

Latchup is a process whereby a parasitic thyristor is triggered by a specific current or voltage. It is useful to know the triggering parameters, to enable comparison between devices and/or to implement safeguards if necessary [16]. In this section, only the “black line” effect is considered. Thus, all the properties are given for the latchup on the line-addressing circuit. The effect does not appear for all ions. Fig. 6 presents the cross-section curve versus LET of the particles. The threshold is between Ar and Kr ions, which places the LET between 15.9 and 40.4 MeV cm²/mg. The number of occurrences is low, giving the cross-section a high uncertainty [17]. It is still preferable to avoid the effect since it does not disappear until power is reset.

The disparity of latchup triggering in the two foundries can not be explained by the design. The tested CISs use similar addressing circuits, and according to the design rules manual the critical minimum distances are the same for the two foundries. However, the epitaxial layer of foundry A is thicker, and the deep substrate has a lower doping level. These two process parameters increase the substrate resistance and explain the increase in SEL sensitivity.

The latchup I-V curves have two particular points: triggering and holding. Implementing safeguards at the system level requires a knowledge of these points. Thanks to the circuit structure, the 3.3V CIS power supply can be modified to allow the measurements of the voltage needed to trigger, and subsequently sustain latchup. The results are summarized in Table III. The voltages recorded gave the same results for ten measurements, so the error depends on the step used (100mV). Twelve measurements of the holding current were taken; Table III shows the mean and standard deviation for each value.

The 1.8V digital circuits are free of latchup effect because the holding voltage is over 1.8V. Thus, only the 3.3V digital circuits are sensitive and need to be protected. The holding current is calculated as the difference between nominal current and the consumption current with one “black line”. As a result, it is not only linked to latchup but also to the increase in consumption due to the white halo. It is relatively high, and can be detected easily if a detection method is needed. Moreover the effects are cumulative if several lines are affected, which means that the protection circuit threshold can be optimized for a given number of defect lines. If the application requires clean frames, the circuit can be operated with a supply below the holding voltage, at the potential cost of degraded electro-optical performance, particularly dynamic, depending on the circuit and the fabrication process. The design of the digital circuits can also be adapted to mitigate latchup. All latchup hardening-by-design techniques can be applied [18], [15], such as operating the whole digital section within a safe supply voltage range (if the holding voltage is known), increasing the distance between PMOS and NMOS transistors, using guard rings, etc.

IV. RESULTS ON SETs

A. Parasitic charge collection

In this section, Single Event Transient effects (SETs) are studied. The power supply to the CIS1 was reset every time current was higher than the nominal value in order to measure the SETs without any degradation caused by the SEL.

Parasitic charge collection was calculated by summing all the charges collected by all the pixels. This value was then

<table>
<thead>
<tr>
<th>Current (mA)</th>
<th>Voltage (V)</th>
</tr>
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<tbody>
<tr>
<td>Triggering point</td>
<td>2.85 ± 0.05</td>
</tr>
<tr>
<td>Holding point</td>
<td>28.46 ± 2.27</td>
</tr>
</tbody>
</table>
compared to the theoretical charge deposited by the particle. SRIM software [19] was used to simulate the charge lost in the dead layer (silicon dioxide with metal layers) and the LET versus the depth in the epitaxial layer. The LET was numerically integrated to obtain the total charge deposited in the epitaxial layer (whose thickness depends on the foundry). The number of charges was obtained by dividing the deposited charge by the mean energy required to create an electron-hole pair in Si: 3.6 eV [20], [21].

Two effects can explain the increased discrepancy. The first is the increased fraction of lost charge due to the blooming effect. Two particles with different LET will not saturate the same number of pixels. Thus, a fraction of the carriers generated by the higher LET particle must diffuse farther before being collected. This fraction undergoes a higher loss due to recombination in the bulk substrate and on surfaces, and collection in transistor nodes (transistors M1, M2, M3). In both effects, the higher the LET, the higher the discrepancy, which is exactly the trend observed in the experiments.

Another consequence of this blooming is a large spread of the SET width. In order to quantify the spread, the anti-blooming is tested in the next section. Two methods are implemented to achieve sensor anti-blooming capabilities.

B. Anti-blooming through the transfer transistor gate

CIS1 and CIS2 do not have a dedicated anti-blooming transistor. However the transfer transistor can act as one, if its lowest voltage is slightly modified. Fig. 8 presents the ideal structure and associated potential. If gate bias is negative, the channel is accumulated, pinning its potential to zero. The electrons cannot cross the potential barrier formed, and the PPD detains the electrons. If the gate is positive, the channel is depleted and the bands are lower in the channel region than around the pinned photodiode. The excess charges inside the PPD are transferred into the sense node (SN).

If the PPD is full of electrons and the transfer transistor gate is slightly positive during integration, the potential of the band underneath the gate is greater than the potential around the PPD. The excess charges therefore move through the channel into the sense node rather than the neighboring photodiode, as displayed in Fig. 8. This reduces or even completely eliminates blooming. In Fig. 9, the SETs are shown for each of the gate biases and for two ions (Ar and Kr).

The anti-blooming method is effective, since the SET spreads less when bias is positive rather than negative. However the drawback is a lower FWC of the PPD, which degrades...
the sensor dynamic [22]. This trend is visible in Fig. 10 where the SET radius decreases with saturation level for increasing voltage values in the lowest transfer gate voltage.

C. Anti-blooming through a dedicated transistor

An anti-blooming transistor behaves in the same way as the transfer gate in the “off” state. It is a dedicated MOS transistor which bends the channel bands to move photodiode excess charges into a node connected to a fixed bias (here 3.3V).

Again the difference is visible in Fig. 11 between negative and positive biases of the transfer gate. The SETs seem narrower than in the previous section because the sensors used here have a much bigger pixel pitch (7 µm), but the decrease in physical scale is the same.

This result shows that an anti-blooming transistor can remove excess charges and the effect of anti-blooming is visible on the SETs even if pixel pitch is greater. As a result, parasitic charge collection is decreased.

The trend is the same for both anti-blooming methods. However, the device commands must be operated carefully if anti-blooming is implemented with the transfer transistor. The excess charges are dumped in the sense node, so it must be properly reset before and after integration time. Otherwise the full sense node will not be able to collect the excess charges coming from the PPD. It is therefore not necessary to add an anti-blooming transistor to reduce parasitic charge collection. The next section will compare the total collected charge for the two anti-blooming capabilities in order to verify that the sense node is an efficient charge collection node for the ion injection level.

D. Total collected charge and blooming

Excess charges removed by the anti-blooming transistor do not appear in the frames. As a result, anti-blooming bias can produce variations in the measured charge. Fig. 13 presents Charge Collection Efficiency (CCE)1 versus gate voltage. The charge collection efficiency is similar for both chips when the voltage is around 0V. However, the value is not at a maximum because the gates are not accumulated. The potential under the gate is still slightly below the equilibrium value and excess charges are still drained into the sense node. If the gates are biased negatively, all the collected parasitic charges are kept in the PPD and they are read in the next frame. On the other hand,

1CCE is defined as the ratio of the charge collected by the device over calculated deposited charge in the device’s epitaxial layer.

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Fig. 9. SETs for different lowest voltage of the transfer gate, obtained with CIS1. White spots mean charge collection in the pixel. Gray scale is not the same for each ion and gate voltage (see the X-cut in Fig. 10).

Fig. 10. SET profiles (X-cut) for each value of the transfer gate lowest voltage, obtained with CIS1. Pixels are 4.5 µm square.

Fig. 11. SETs for each anti-blooming gate voltage, obtained with CIS1. White spots mean charge collection in the pixel. Gray scale is not the same for each ion and gate voltage (see the X-cut in Fig. 12).
Fig. 12. SET profiles (X-cut) for each value of the transfer gate lowest voltage, obtained with CIS3. Pixels are 7 µm square.

Fig. 13. Charge collection efficiency versus gate voltage for CIS1 (lowest transfer gate voltage) and CIS3 (dedicated anti-blooming transistor).

for positive bias, the excess collected charges flow through the anti-blooming transistor (or TG) and are drained in the pixel supply. Thus, minimizing the number of pixels affected by SETs requires the use of a positive bias on the anti-blooming gate (or TG). It is worth mentioning that in some applications such as particle detection, it may be desirable to negatively bias the TG so as to measure the entire collected charge (and to avoid charge dumping in the supply voltage).

The collection of the parasitic charges for the saturated pixels is lower if anti-blooming is activated. The result is a decrease in the FWC for all the saturated pixels. Since an SET has mainly saturated pixels, the CCE is closely related to the Full Well Capacity of the photodiode. Thus, the CCE decrease follows the transistor gate bias increase (for both anti-blooming and transfer transistors) [23].

For \( V_g < -0.3\, \text{V} \), FWC is constant. As a result, the gate voltage does not produce any variations in the CCE. However, the LET of the particle has an effect, since the two plateau values are different.

For \( V_g > -0.3\, \text{V} \), anti-blooming is active. FWC is reduced, and excess charges are carried away by the sense node (or anti-blooming node). As a result, the total collected charge starts a non-linear decrease, which can be explained by the inversion regime of the MOS gate (from weak to moderate inversion).

V. CONCLUSIONS

Single Event Effects (SEEs) in 4T and 5T CMOS image sensors (CISs) have been investigated throughout the paper. Effects of heavy ion irradiation include SEL and SET.

The observed SEL is an effect occurring in the level shifter of the addressing sections of the device, but only on one of the two foundries tested. If the technology has not been tested in the worst case conditions, the circuit has to be protected or the effects mitigated. Depending on the mission requirements, the protection can be an automatic power reset circuit (at the cost of down time) or specific hardening to latchup through operational or design parameters. In either case, latchup properties must be known. In the device used here, frames can be completely corrupted by addressing errors. One of the hardening methods is the operation of the digital supply under the SEL holding voltage.

Once the CIS is operational, Single Event Transient (SET) events still appear with each ion generating charges, which form white circles on the frames. These charges are collected both by diffusion and blooming. Since the pinned photodiodes used here have a lower FWC than the readout chain saturation level, blooming has a visible effect on frames. As a result,
SETs can be slightly reduced for the application by using the anti-blooming capability of the sensor. Anti-blooming can be used in all 4T CISs through the lower voltage level of the transfer transistor gate. In this case the sense node needs to be reset before and after (or during) the integration time. A dedicated anti-blooming transistor can also be used with similar results, without the need to add specific reset of the sense node during integration (still needed before the PPD charge transfer). It is interesting to note that if pinned photodiode CISs were used for charged particle detection, it would be necessary to bias the TG negatively during integration to maximize the number of charges seen on the output. The opposite effect can be achieved through a zero or positive gate bias. The anti-blooming effectively reduces the SET spread and the total measured charge for an SET. It can thus be useful for both space and nuclear environments to minimize sensor perturbations, especially where radiation flux is high as found in the Inertial Confinement Fusion (ICF) facilities. Moreover it can be adapted in real time for dynamic radiation fields (solar flares, radiation belts, etc), if the system design allows supply voltage variations. The drawback of this operation is a dynamic level degradation, which is why a trade-off is necessary.

APPENDIX A
DESCRIPTION OF THE TWO-COLUMN READOUT CIRCUIT INDUCED BY THE SEL

When selection signals are low, the corresponding PMOS transistors act like perfectly closed switches. The two other transistors first operate in a sub-threshold region for low illumination cases. Drain current of the transistors is given by Eq. 1 [24].

$$I_D = \frac{W}{L} I_0 \exp \left( \frac{V_G - V_M}{n \beta} \right) \left[ 1 - \exp \left( \frac{V_D}{\beta} \right) \right]$$  (1)

Where $\beta = kT/q$ and $k$ is the Boltzmann constant, $T$ is temperature, and $q$ is the electron charge. $W$ and $L$ are the transistor width and length, respectively. $I_0$ is a process parameter. $V_G$ and $V_D$ are the gate and drain voltages of the transistors, respectively. $V_M$ is the upper limit of the weak inversion voltage, and $n$ is a parameter between 1 and 1.5 which barely varies with $V_G$.

This can be simplified by dividing the equation of the input transistor by the one of the latched transistor. If the transistors match, the result is given in Eq. 2

$$\frac{I_1}{I_2} = \exp \left( \frac{V_1 - V_2}{n \beta} \right)$$  (2)

This equation can be reformulated with the node current law $I_c = I_1 + I_2$ giving Eq. 3, and its symmetrical equation for $I_1$.  

$$I_2 = I_c \frac{1}{1 + \exp \left( \frac{V_1 - V_2}{\beta} \right)}$$  (3)

A zero voltage difference gives the same current $I_2$ for both $I_1$ and $I_2$. This result is consistent with the fact that both column readout circuits are the same (without taking mismatch between transistors into consideration). When the two gate voltages are different, Fig. 14 shows that the input current ratio is one order of magnitude higher for every 60mV at room temperature (300K).

Fig. 14. Current ratio for the difference between input voltages $V_1 - V_2$.

As a result, the structure can be considered as a “winner-takes-all”. When one of the inputs is higher, current passes through the branched concerned and the output signal is only determined by this signal. However when input signals are nearly equal, the voltage output is a mean of the two input signals.

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